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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,813	09/24/2003	Ramanand Venkata	ALT-282	7626

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,813	VENKATA ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16* is/are allowed.

6)☒ Claim(s) *1-7,10-13,17,19,22,24,25 and 27* is/are rejected.

7)☒ Claim(s) *8,9,14,15,18,20,21,23 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is responsive to the amendment filed on January 27, 2006. Claims 1-27 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 10, 17, 19, 22, 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henkel U.S. Patent 6,055,644 in view of Munday et al. U.S. Patent 4,025,865.

4. As per claim 1, Henkel teaches a serial interface for use in a programmable logic device[1], said serial interface comprising:

a plurality of channels [20aa....zz fig. 2a], each of the channels including at least transmit circuitry [fig. 2b, 3b, 5b disclose the circuitry for transmit clock signal];

central control circuitry including at least one clock source [40 fig. 1] for generating at least one transmit clock for use by the transmit circuitry in each of the channels [col. 3 lines 11-25], each the transmit clock having a respective first clock rate [inherent-col. 3 lines 47-50].

clock circuitry in a plurality of the channels for providing from at least one the transmit clock a channel-derived clock having a second clock rate at most equal to the respective first clock rate [col. 3 lines 38-41 and claim 7- modifying the channel clock of the respective channel;

col. 2 lines 1-5 show at most the second clock rate is equal to the respective first clock rate], the clock circuitry in each of the plurality of channels being controllable independently of the clock circuitry in any other of the plurality of channels [col. 3 lines 27-31; abstract].

Henkel teaches a mean in each channel to generate a channel clock signal from the central master clock signal. However, Henkel does not explicitly teach a division circuitry provided in each channel in order to generate the channel clock.

Munday et al. teach another method for synthesizing signal data in multiple channel. Specifically, Munday et al. teach a frequency signaling circuit includes a plurality of channels, each channel having division means for frequency division of a clock signal from a central clock circuit [5 fig. 1] wherein each division circuitry is being independently control [abstract].

At the time of the invention was made, it would having obvious to one of ordinary skill in the art to have modified the circuitry of Henkel with the frequency division circuitry of Munday et al. to generate a second clock rate in each channel since the frequency/clock division circuitry is such an old and well-know circuit in the art for modifying clock rate.

5. As per claim 2, Munday et al. teach each of the channels includes the clock division circuitry [abstract].

6. As per claim 3, Although not explicitly taught in Henkel or Munday et al., that the respective first divider selectably divides the respective first clock rate by one of a group of at least one integer value. However, because Henkel or Munday et al. does not explicitly prohibit

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[1] Henkel teach a system that can be applied to any multi-channel architecture [col. 4 lines 14-18].

the divider from selectively divide the first clock rate by one of integer value and because the division by an integer in the clock divider circuit is such a well know means to modify the clock rate, it would have been obvious by design choice to modify the clock rate of Henkel-Munday system by using one of a group of at least one integer value.

7. As per claim 5, Henkel teach a the modifying of the clock rate is selected by user programming of the programmable logic device [col. 5 lines 6-8].

8. As per claim 6, obvious.

9. As per claim 7, obvious.

10. As per claim 10, Henkel teaches the at least one clock source consists of a single clock source [40 fig. 5a] generating a single transmit clock having a single transmit clock rate.

11. As per claim 17, Henkel and Munday et al. does not explicitly teach the programmable logic device comprising the serial interface, however, Henkel teaches a device that capable of connecting to one or more individual DUT. Therefore, it is obvious to one of ordinary skill in the art that Henkel's generic interface included the claimed serial interface since the special interface does not effect the fundamental function of Henkel's system.

12. As per claim 19, APA.

13. As per claim 22, repletion of claim 17.

14. As per claim 24, obvious.

15. As per claim 25, the system is well know in the art of computer architecture.

16. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henkel/Munday et al. as applied to claim 1 above, and further in view of Swoboda et al. U.S. 5,903,746.

17. As per claim 11, Henkel/Munday et al. only teach one clock source. However, Swoboda et al. teach another clock acquisition subsystem for a data processing system has an interlocked clock multiplexer for acquiring a clock source which is provided as clock signal to the data processing system. Specifically, Swoboda et al teach the at least one clock source comprises a plurality of clock sources, each of the clock sources generating its own respective first clock rate [col. 2 lines 6-11; col. 3 lines 9-20].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Henkel/Munday et al. with the multiple clock sources as taught by Swoboda et al. in order to optimized the operation of the system [col. 3 lines 26-32].

18. As per claim 12, Swoboda et al. teach a selector for selecting one of the plurality of clock sources [col. 3 lines 29-38] and

it would have been obvious to one of ordinary skill that the combine teachings of Henkel/Munday et al. and Swoboda et al. teach the selecting of the plurality of clock sources and output of the clock division circuitry.

19. As per claim 13, Swoboda et al. teach the selector comprises a multiplexer [100 fig. 1].

20. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted of Prior Art (APA) in view of Henkel and Munday et al..

21. As per claim 27, APA teaches a programmable logic device comprising:

a programmable logic core; and

serial interface means comprising:

a plurality of channel means, each of the channel means including a least transmit means;

a central control circuitry including at least one clock source for generating at least one transmit clock for used by the transmit circuitry in each of the channels, each the transmit clock having a respective first clock rate [paragraph 0002 – Spec.] However, APA does not teach clock division circuitry in at least one of the channels for providing from at least one transmit clock a channel-derived clock having a second clock rate at most equal to the respective first clock rate.

Henkel teaches another multi-channel architecture [fig. 5a] comprising a central master clock generator for generating a central master clock signal for used by the transmit circuitry in each of the channels [col. 3 lines 11-25; col. 4 lines 14-18]. Specifically, Henkel teaches a clock circuitry in a plurality of the channels for providing from at least one the transmit clock a channel-derived clock having a second clock rate at most equal to the respective first clock rate [col. 3 lines 38-41 and claim 7- modifying the channel clock of the respective channel; col. 2 lines 1-5 show at most the second clock rate is equal to the respective first clock rate], the clock

circuitry in each of the plurality of channels being controllable independently of the clock circuitry in any other of the plurality of channels [col. 3 lines 27-31; abstract].

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of APA with each channel having a separate clock circuitry as taught by Henkel in order to allow each channel the ability to operate independently and at different clock rate [col. 3 lines 20-25].

Henkel teaches a mean in each channel to generate a channel clock signal from the central master clock signal. However, Henkel does not explicitly teach a division circuitry provided in each channel in order to generate the channel clock.

Munday et al. teach a frequency division circuit [see discussion in claim 1].

Allowable Subject Matter

22. Claim 16 allowed.

23. Claims 8-9, 14-15 18, 20-21, 23, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran

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